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1 **Oversampling parallel delta-sigma modulator A/D conversion**
Galton, I.; Jensen, H.T.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactic [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volu 43 , Issue: 12 , Dec. 1996
Pages:801 - 810

[Abstract] [PDF Full-Text (1204 KB)] **IEEE JNL**

---

2 **A 16X oversampling CMOS ADC with 100 kHz bandwidth and 90dB S**
Dedic, I.J.;
Advanced A-D and D-A Conversion Techniques and their Applications, 1994. Second International Conference on , 6-8 Jul 1994
Pages:82 - 89

[Abstract] [PDF Full-Text (332 KB)] **IEE CNF**

---

3 **An overview of sigma delta ADCs and DAC devices**
Stewart, R.W.;
Oversampling and Sigma-Delta Strategies for DSP, IEE Colloquium on , 23 No 1995
Pages:1/1 - 1/9

[Abstract] [PDF Full-Text (576 KB)] **IEE CNF**

---

4 **Deterministic analysis of oversampled A/D conversion and decoding improvement based on consistent estimates**
Thao, N.T.; Vetterli, M.;
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Sigr

Processing, IEEE Transactions on] , Volume: 42 , Issue: 3 , March 1994
Pages:519 - 531

[Abstract] [PDF Full-Text (1088 KB)] IEEE JNL

---

5 **A 14-bit 500 kHz delta-sigma ADC with 16 times oversampling**
Baird, R.T.; Fiez, T.S.;
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995 , May 1995
Pages:199 - 202

[Abstract] [PDF Full-Text (536 KB)] IEEE CNF

---

6 **A high-speed high-resolution oversampled A/D converter**
Burra, G.; Chao, K.S.;
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on , 3-6 May 1993
Pages:1282 - 1285 vol.2

[Abstract] [PDF Full-Text (324 KB)] IEEE CNF

---

7 **Improved performance of multi-bit delta-sigma analog to digital converters via requantization**
Harris, F.; Brooking, E.; McKnight, B.;
Circuits and Systems, 1991., IEEE International Sympoisum on , 11-14 June 1
Pages:1629 - 1632 vol.3

[Abstract] [PDF Full-Text (260 KB)] IEEE CNF

---

8 **A single shot ΣΔ architecture for multiplexed applications**
Lyden, C.; Ryan, J.; Ugarte, C.A.; Kornblum, J.; Fan Ma Yung;
Oversampling and Sigma-Delta Strategies for DSP, IEE Colloquium on , 23 No 1995
Pages:6/1 - 6/4

[Abstract] [PDF Full-Text (228 KB)] IEE CNF

---

9 **A DNL measurement on an oversampling noise shaping ADC**
Goudie, A.G.; Story, M.J.;
Advanced A-D and D-A Conversion Techniques and their Applications, 1994. Second International Conference on , 6-8 Jul 1994
Pages:181 - 185

[Abstract] [PDF Full-Text (204 KB)] IEE CNF

---

10 **On the performance of an oversampled analog to digital converter digital requantizer in feedback path**
Harris, F.; McKnight, B.; Constantinides, T.;
Analogue to Digital and Digital to Analogue Conversion, 1991., International Conference on , 17-19 Sep 1991
Pages:17 - 22

[Abstract] [PDF Full-Text (340 KB)] IEE CNF

---

11 **An efficient /spl Delta//spl Sigma/ ADC architecture for low oversampling ratios**
Markus, J.; Temes, G.C.;
Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circuit Systems I: Fundamental Theory and Applications, IEEE Transactions on] , Vol 51 , Issue: 1 , Jan. 2004
Pages:63 - 71

[Abstract] [PDF Full-Text (304 KB)] IEEE JNL

---

12 **Oversampled Sigma-Delta Modulation**
Gray, R.;
Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 35 , Iss 5 , May 1987
Pages:481 - 489

[Abstract] [PDF Full-Text (864 KB)] IEEE JNL

---

13 **A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delt sigma modulation at 8× oversampling ratio**
Fujimori, I.; Longo, L.; Hairapetian, A.; Seiyama, K.; Kosic, S.; Jun Cao; Shu-Chan;
Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 12 , Dec. 2000
Pages:1820 - 1828

[Abstract] [PDF Full-Text (184 KB)] IEEE JNL

---

14 **A low oversampling ratio 14-b 500-kHz ΔΣ ADC with a self-calibrat multibit DAC**
Baird, R.T.; Fiez, T.S.;
Solid-State Circuits, IEEE Journal of , Volume: 31 , Issue: 3 , March 1996
Pages:312 - 320

[Abstract] [PDF Full-Text (1192 KB)] IEEE JNL

---

15 **A 13-b 10-Msample/s ADC digitally calibrated with oversampling d sigma converter**
Tzi-Hsiung Shu; Bang-Sup Song; Bacrania, K.;
Solid-State Circuits, IEEE Journal of , Volume: 30 , Issue: 4 , April 1995
Pages:443 - 452

[Abstract] [PDF Full-Text (960 KB)] IEEE JNL

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1 Session 9: Oversampled gain-boosting

Omid Oliaei

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(194.94 KB) Additional Information: full citation, abstract, references, index terms

A dynamic gain-enhancement technique suitable for lowvoltage low-power oversampling circuits, particularly sigma-delta converters, is presented. This method makes use of a discrete time integrator to improve gradually the output resistance of the main amplifier over successive clocks.

Keywords: ADC, DAC, MOS amplifier, OTA, bootstrapping, gain boosting, gain enhancement, sigma-delta, switched-capacitor

2 Low-voltage low-power switched-current circuits and systems

Nianxiong Tan, S. Eriksson

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Full text available: pdf(642.50 KB) Publisher Site Additional Information: full citation, abstract

This paper presents low-voltage low-power switched-current circuits and systems. Novel class AB configuration and common-mode feedforward are the essence. A delay line, memory cell, oversampling A/D converter, and chopper-stabilized oversampling A/D converter were designed and implemented. Measurement results are presented as well.

Keywords: CMOS IC, CMOS analogue integrated circuits, LV switched-current circuits, SI memory cell, analogue processing circuits, analogue storage, analogue-digital conversion, chopper-stabilized oversampling ADC, class AB configuration, common-mode feedforward, delay line, delay lines, feedforward, low-power switched-current circuits, oversampling A/D converter, sampled data circuits, switched current circuits

3 Top-down design of a xDSL 14-bit 4MS/s sigma-delta modulator in digital CMOS technology

R. del Rio, J. de la Rosa, F. Medeiro, B. Pérez-Verdú, A. Rodriguez-Vázquez

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(149.63 KB) Additional Information: full citation, references, index terms

4 Substrate crosstalk analysis in mixed signal CMOS integrated circuits: embedded tutorial

Makoto Nagata, Atsushi Iwata

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(476.00 KB) Additional Information: full citation, references

5 Analog synthesis & design methodology: Optimal design of delta-sigma ADCs by design space exploration

Ovidiu Bajdechi, Johan H. Huijsing, Georges Gielen

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(191.40 KB) Additional Information: full citation, abstract, references, index terms

An algorithm for architecture-level exploration of &SGR;D ADC design space is presented. The algorithm finds an optimal solution by exhaustively exploring both single-loop and cascaded architectures, with single-bit or multi-bit quantizer, for a range of oversampling ratios. A fast filter-level step evaluates the performance of all loop-filter topologies and passes the accepted solutions to the architecture-level optimization step which maps the filters on feasible architectures and evaluates th ...

Keywords: ADC, CAD, delta-sigma

6 Low-power sensing and digitization of cardiac signals based on sigma-delta conversion (poster session)

Andrea Gerosa, Arianna Novo, Andrea Neviani

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Full text available: pdf(245.92 KB) Additional Information: full citation, abstract, references, index terms

In this work we propose an architecture for the acquisition and digitization of cardiac signals in a pace-maker, based on &Sgr;&Dgr; modulation. Due to the characteristics of such an application, the proposed system presents the typical design challenges of low-voltage, low-power circuits. The work demonstrates that, thanks to the narrow bandwidth typical of biological signals (50-150 Hz), oversampling conversion techniques can be advantageous in terms of power di ...

7 Analog design space exploration: Architectural selection of A/D converters

Martin Vogels, Georges Gielen

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(139.39 KB) Additional Information: full citation, abstract, references, index terms

A method for the architectural selection of analog to digital (A/D) converters based on a generic figure of merit is described. First a figure of merit for the power consumption is introduced. This figure of merit includes both target specifications and technology data and has five generic parameters. The values of these generic parameters can be estimated by analyzing the different converter structures or by means of a fitting procedure using data from published designs. It is shown that the ge ...

Keywords: A/D conversion, power estimation

8 (Special session) presentation + poster disscussion: university design contest: A dynamic element matching circuit for multi-bit delta-sigma modulators
Ryozo Katoh, Shin-ya Kobayashi, Takao Waho
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**
Full text available: pdf(161.73 KB) Additional Information: full citation, abstract, references

A 30k-gate dynamic element matching circuit for bandpass modulators with a 4-bit quantizer is designed by using 0.35-μm CMOS technology. Second-order bandpass mismatch-shaping algorithm improves the signal-to-noise ratio by ~30dB (~5 bit). The core circuit area and the estimated operation speed were 1.44 mm² and 20 MHz, respectively.

9 Mixed-signal design and simulation: A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference
Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, Keith L. Kraver, Matthew R. Guthaus, Richard B. Brown
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(793.60 KB) Additional Information: full citation, abstract, references, citings, index terms

In this work, we report on an unprecedented design where digital, analog, and MEMS technologies are combined to realize a general-purpose single-chip CMOS microsystem. The convergence of these technologies has enabled the development of a low power, portable microinstrument ideally suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methodology, inductor, low power, low voltage analog, microcontroller, microsystem, mixed-signal, system-on-chip, varactor

10 Detection of defective sensor elements using ΣΔ -modulation and a matched filter
D. Weiler, O. Machul, D. Hammerschmidt, B. J. Hosticka
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(88.57 KB) Additional Information: full citation, references, index terms
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11 On the optimum design of regulated cascode operational transconductance amplifiers
Thomas Burger, Qiuting Huang
August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**
Full text available: pdf(710.23 KB) Additional Information: full citation, abstract, references, index terms

An optimal design procedure to achieve minimum power consumption for a given technology and gain bandwidth is presented. Regulated cascode gain enhancement is used to ensure sufficient DC-gain at minimum gate length transistors. To validate the approach five folded cascode OTA's have been implemented, spanning a bias range of 1μA - 10mA, with measured unity-gain bandwidths within 20% of the designed value. For 17 mW at 3 V, a 0.5 μm

12 Session 4B: high-level design tools for analog circuits: Verification of delta-sigma converters using adaptive regression modeling
Jeongjin Roh, Suresh Seshadri, Jacob A. Abraham

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(116.40 KB) Additional Information: full citation, abstract, references

A new verification technique for ΔΣ analog-to-digital converters (ADC) is proposed. The ADC is partitioned into functional blocks, and adaptive regression models for each partition are constructed using transistor-level simulation data. Non-idealities in circuit behavior are captured by the adaptive regression technique from the collected data. The algorithms have been implemented in a simulation program ARSIM (Adaptive Regression Simulator), which performs data sampling, model build ...

13 Session 4B: high-level design tools for analog circuits: DAISY: a simulation-based high-level synthesis tool for ΔΣ modulators

K. Francken, P. Vancorenland, G. Gielen

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(240.09 KB) Additional Information: full citation, abstract, references, citings

An integrated tool called DAISY (*D*elta-Sigma *A*nalys*i*s and *Sy*nthesis) is presented for the high-level synthesis of ΔΣ modulators. The approach determines both the optimum modulator topology and the required building block specifications, such that the system specifications -- mainly accuracy and signal bandwidth -- are satisfied at the lowest possible power consumption. A genetic-based differential evolution algorithm is used in combination with a fast dedi ...

14 TAM Optimization for Mixed-Signal SOCs using Analog Test Wrappers

Anuja Sehgal, Sule Ozev, Krishnendu Chakrabarty

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(167.79 KB) Additional Information: full citation, abstract, citings, index terms

We present a new approach for TAM optimization and testscheduling in the modular testing of mixed-signal SOCs. A testplanning approach for digital SOCs is extended to handle analogcores in a plug-and-play fashion. A test wrapper based on anADC/DAC pair and a digital configuration circuit is designed foranalog cores such that these cores can be accessed through digitalTAMs. In this way, there is no dependence on an analog testbus and expensive mixed-signal testers. Experimental results arepresent ...

15 CAD: Synthesis of continuous-time filters and analog to digital converters by integrated constraint transformation, floorplanning and routing

Hua Tang, Hui Zhang, Alex Doboli

April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**

Full text available: pdf(174.45 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a layout-aware analog synthesis methodology. The methodology includes parameter exploration and classification, parameter domain pruning and sampling, and identification of parameter dependencies. The optimization process executes a combined constraint transformation, floorplanning and global routing. The paper presents results for a high frequency continuous-time filter, and two □Δ ADCs. Compared to similar work, the methodology is more flexible in handling new de ...

Keywords: □Δ modulator, continuous-time filter, synthesis

16 A 1.5V low-power third order continuous-time lowpass ΣΔ A/D converter (poster

session)
Friedel Gerfers, Yiannos Manoli
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Full text available: pdf(222.84 KB) Additional Information: full citation, abstract, references, index terms

This paper presents the design of a 3rd-order lowpass &Sgr;&Dgr; g-to-digital (A/D) converter using a continuous-time(CT) loopfilter. The loopfilter has been implemented by using active RC-integrators. The influence of the low supply voltage on the building blocks such as the amplifier and the common mode feedback as well as on the overall &Sgr;&Dgr modulator is discussed. Simulation results of the 1.5V CT &Sgr;&Dgr; A/D converter show a 75 dB dynamic range in a bandwidth of ...

17 A sigma-delta modulation based BIST scheme for mixed-signal circuits
Jiun-Lang Huang, Kwang-Ting Cheng
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
Full text available: pdf(117.31 KB) Additional Information: full citation, references, citings

18 A new built-in self-test approach for digital-to-analog and analog-to-digital converters
Karim Arabi, Bozena Kaminska, Janusz Rzeszut
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(395.28 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper proposes a test approach and circuitry suitable for built-in self-test (BIST) of digital-to-analog (D/A) and analog-to-digital (A/D) converters. Offset, gain, linearity and differential linearity errors are tested without using test equipment. The proposed BIST structure decreases the test cost and test time. The BIST circuitry has been designed to D/A and A/D converters using CMOS 1.2 &mgr;m technology. By only a minor modification the test structure would be able to localize th ...

19 A new algorithm for the design of stable higher order single loop sigma delta analog-to-digital converters
S. R. Kadivar, D. Schmitt-Landsiedel, H. Klar
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(341.91 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

Abstract: This paper presents a new algorithm to attain optimized network scaling in single loop, 1 bit Sigma Delta Analog 1d Digital Converters (SD ADC) of order three or more. The algorithm is based on a novel mathematical description of stability and performance criteria of the SD ADC and on the application of nonlinear interactive optimization techniques. The feasibility of the new algorithm has been confirmed in practical implementations. The method brings new insight on the correlation bet ...

Keywords: CAD, SD ADC, analogue-digital conversion, convertors, electronic engineering computing, higher order, network scaling, nonlinear interactive optimization, performance criteria, sigma delta analog-to-digital converters, single loop

20 Low power high speed analog-to-digital converter for wireless communications

A. E. Hussein, M. I. Elmasry
March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**

Full text available: pdf(271.91 KB) Additional Information: full citation, abstract, references, index terms

A new ADC architecture is devised. This architecture is memory based, in which the last sample is used to predict the current one, resulting in both power dissipation and energy reduction. The low power dissipation is a vital factor when we consider the chip reliability and integrity. The low energy consumption is a critical factor when we deal with battery operated devices like PCSs. This technique may also be used to extend the attainable flash converter resolution by pre-calculating the mo ...

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